Low frequency noise studies on AlGaN/GaN HEMTS with off-state stress beyond the critical voltage

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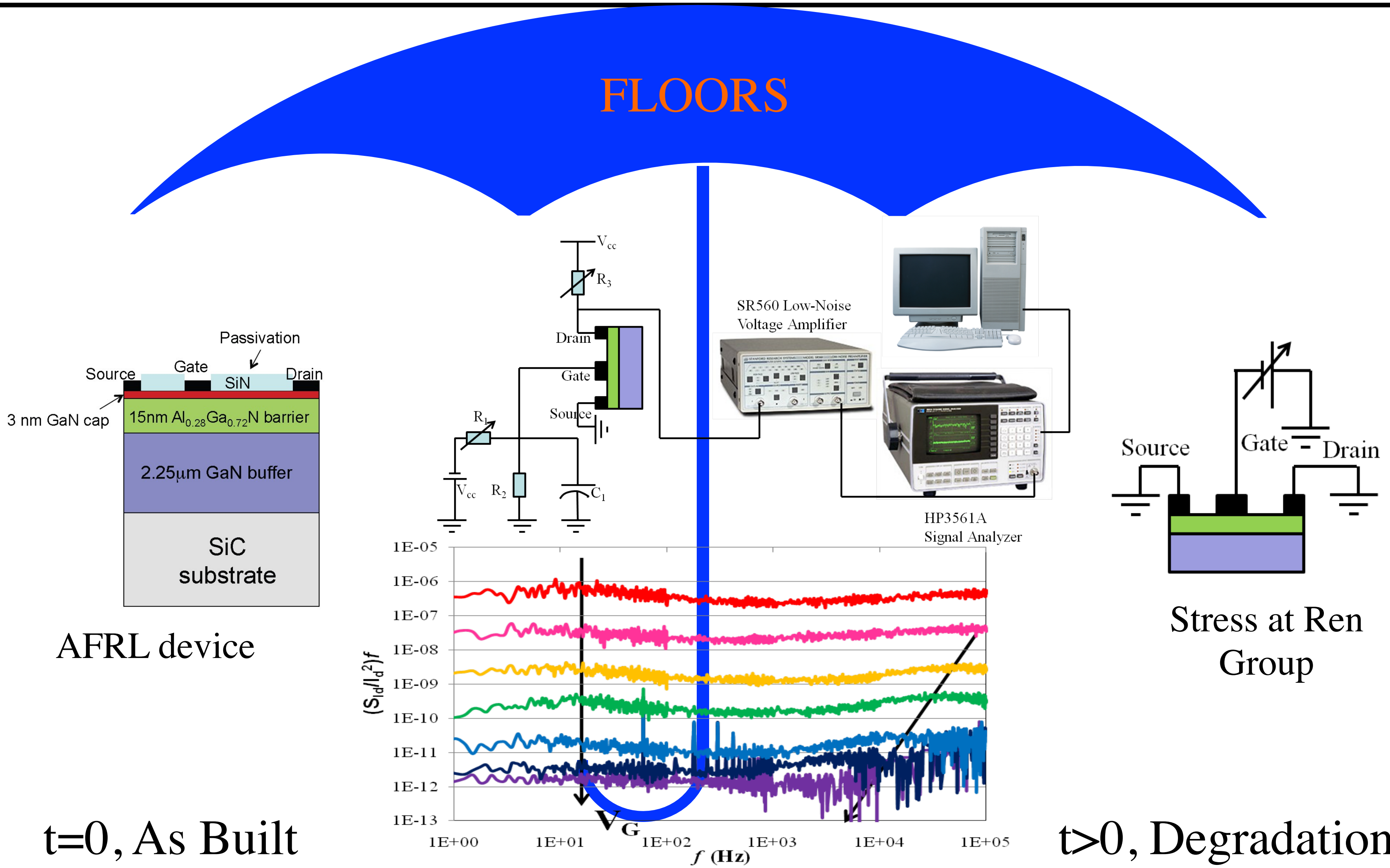
FLOORS
Passivation
Source
Gate
SiN
Drain
3 nm GaN cap
15nm Al0.28Ga0.72N barrier
2.25µm GaN buffer
SiC substrate
AFRL device
Vcc
R3
Drain
Gate
Source
R1
Vcc
R2
C1
SR560 Low-Noise Voltage Amplifier
HP3561A Signal Analyzer
(Sid/Id2)f
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E+00
1E+01
1E+02
1E+03
1E+04
1E+05
f (Hz)
VG
Source
Gate
Drain
Stress at Ren Group
t=0, As Built
t>0, Degradation

Outline

- Off-state Stress Beyond The Critical Voltage
- Channel Noise Measurement and Analysis
- Gate Noise Measurement and Analysis
- Conclusions

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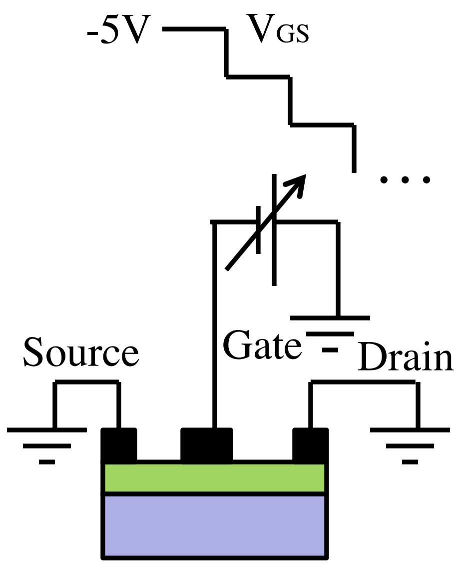
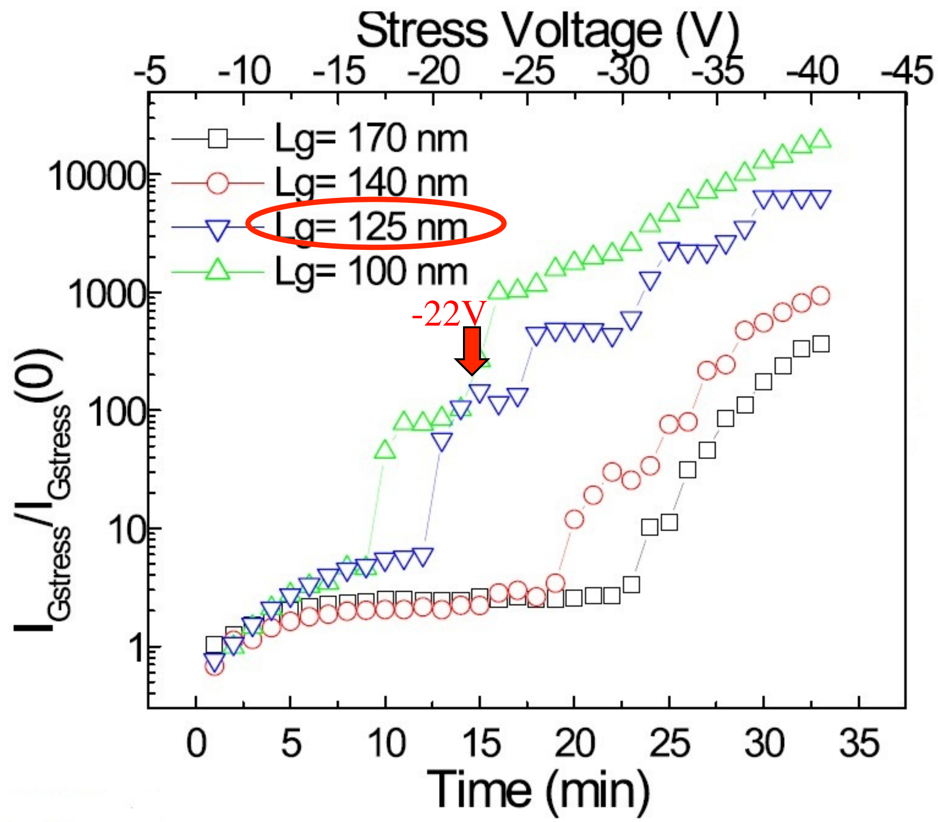
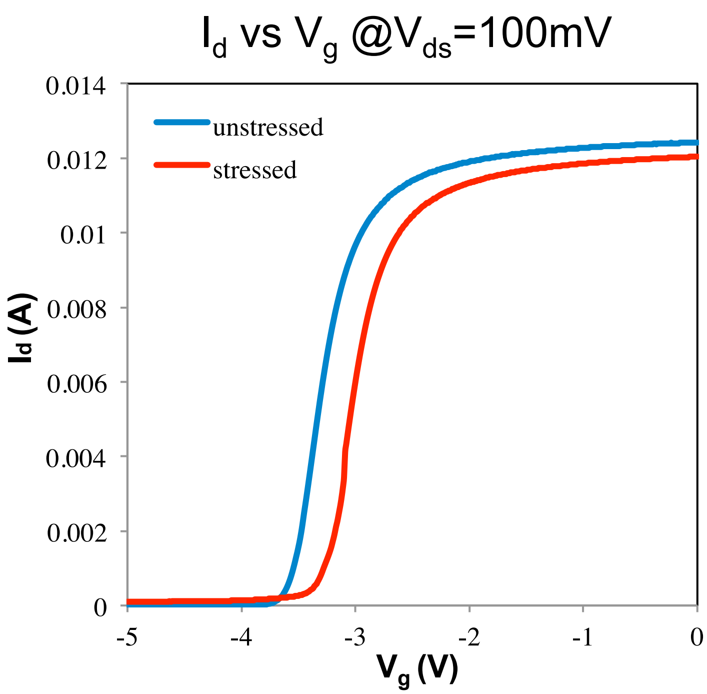
Off-state stress conditions

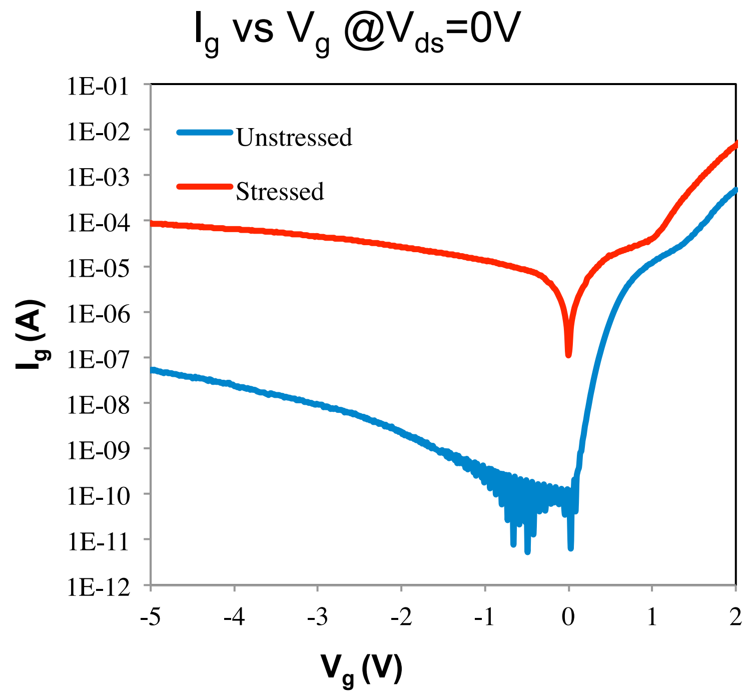
Ren group: V_{GS} step biased from -5V to beyond the critical voltage (-22V for 125nm gate length device) in -1 step while source and drain were grounded.





DC Characteristic before and after stress





- Threshold shift (from -3.6V to -3.4V)
- Leakage current increases by 3 orders(from 10^{-8} A to 10^{-5} A)

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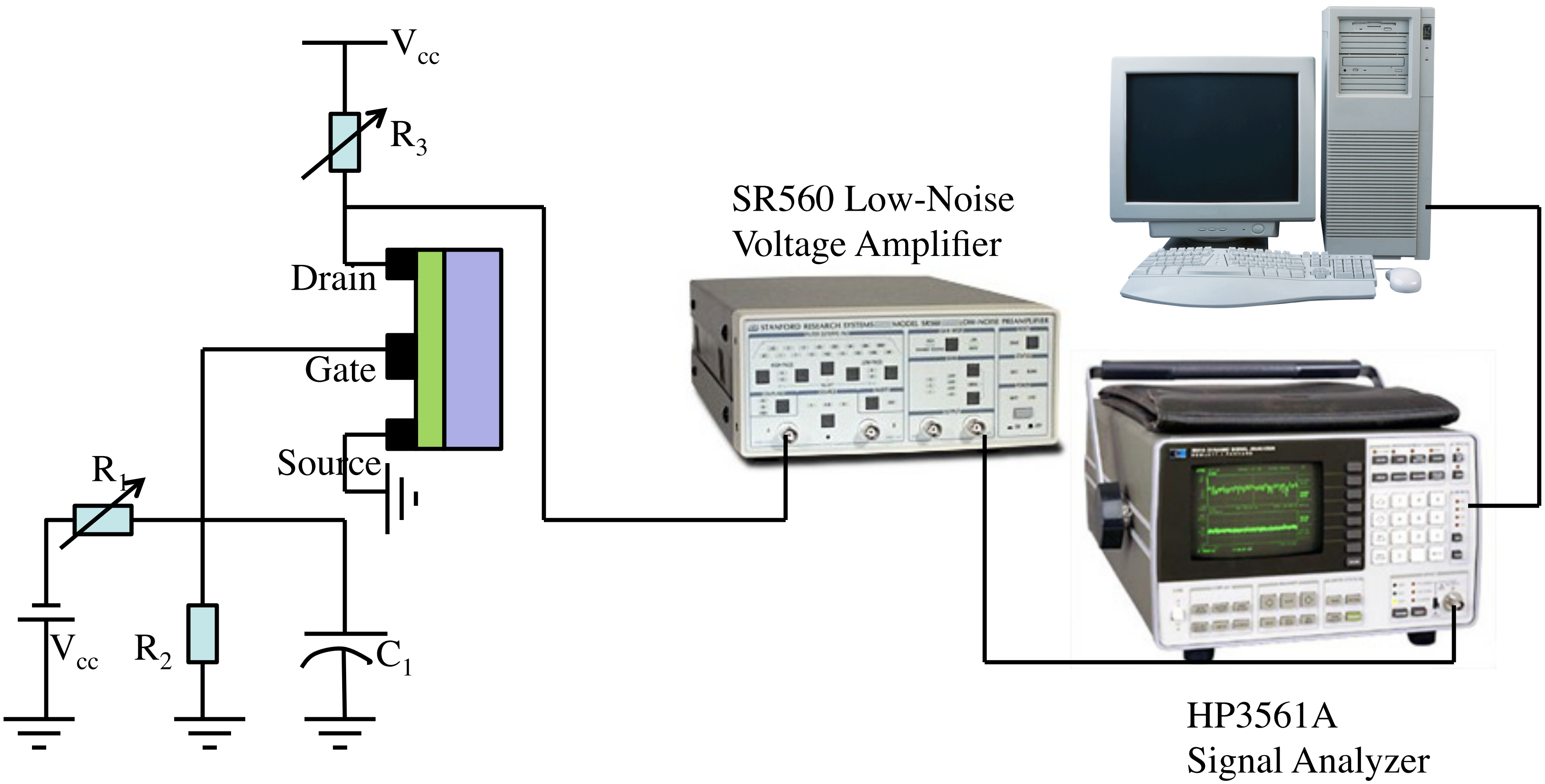
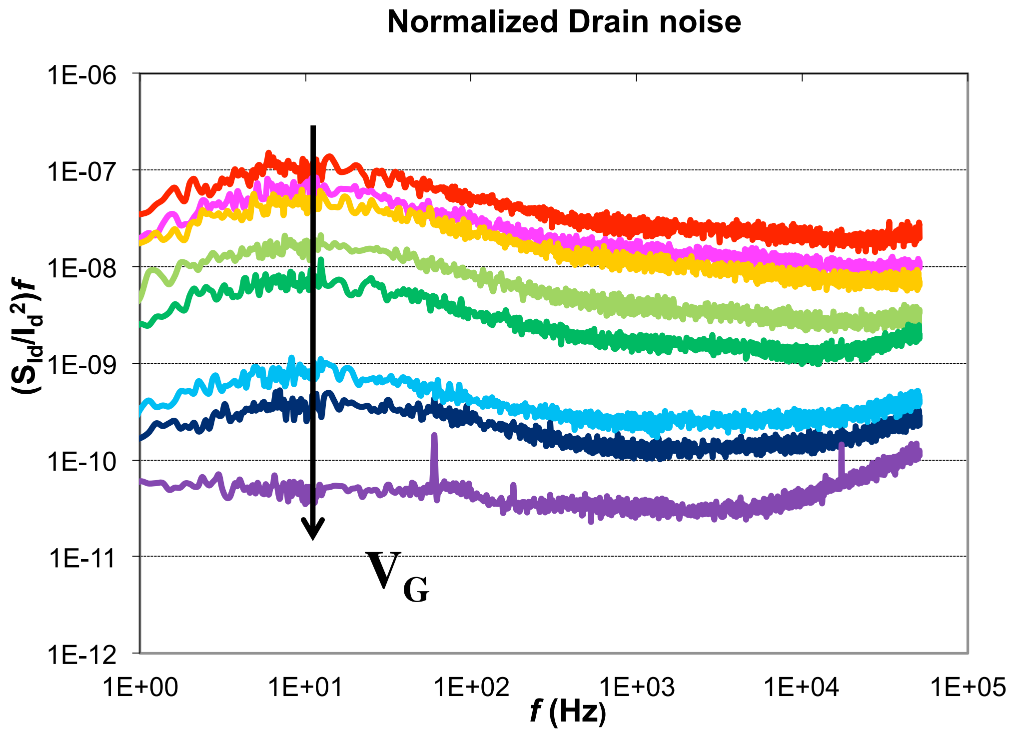
Channel Noise Measurement Setup

Keep V_{ds}=100mV during the measurement. V_{gs} bias ranges from -3.4V to -1V.

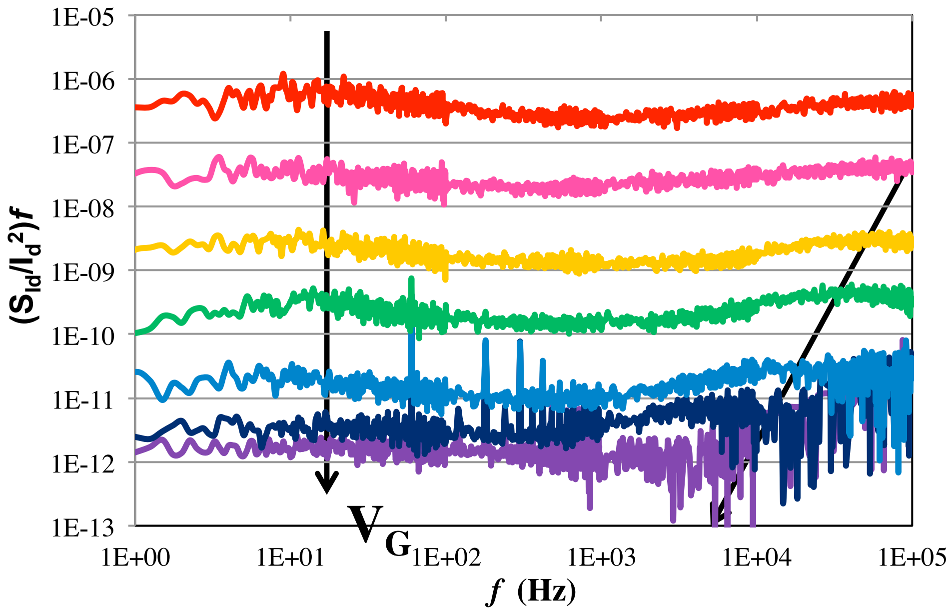


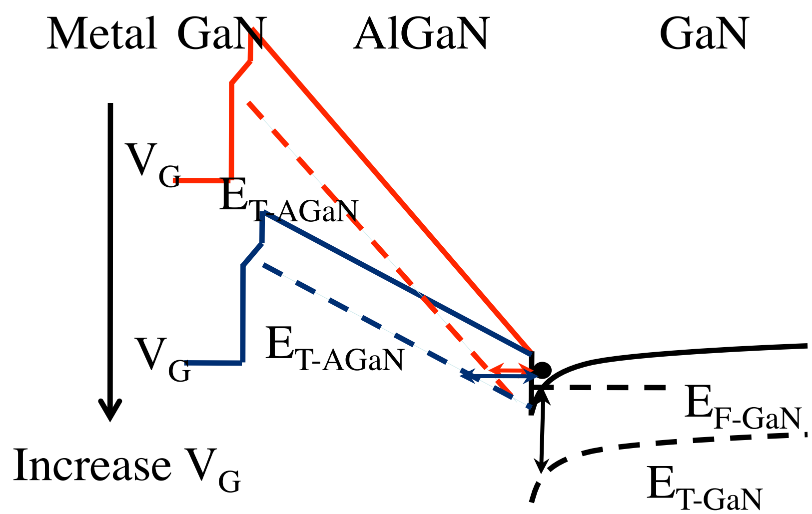
Channel Noise Of Virgin Device



- Lorentzian observed at 10Hz.
- No GR noise component at higher gate bias indicating that the GaN buffer trap is in the gated part of the channel.

Channel Noise Of Stressed Device





- Additional Lorentzian was observed around 3kHz.
- Characteristic f varying with V_G indicating trap is in the AlGaN side at the channel interface.
- The bump at 10Hz becomes smooth indicating the increase on the overall channel noise level.

1/*f* Noise Model Of Channel Noise

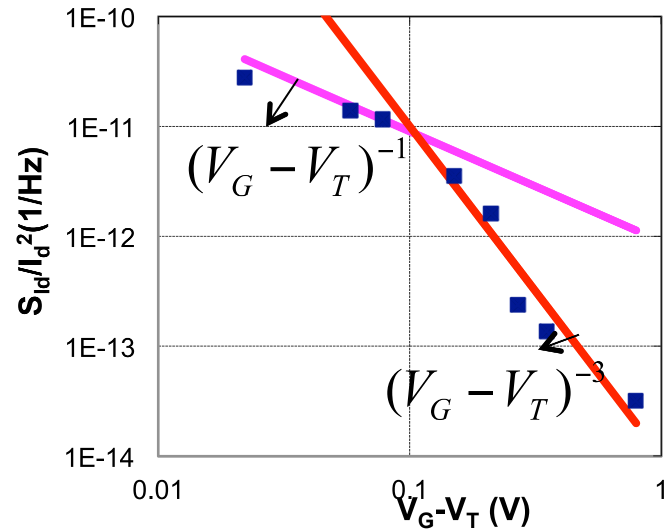
- Carrier number fluctuations

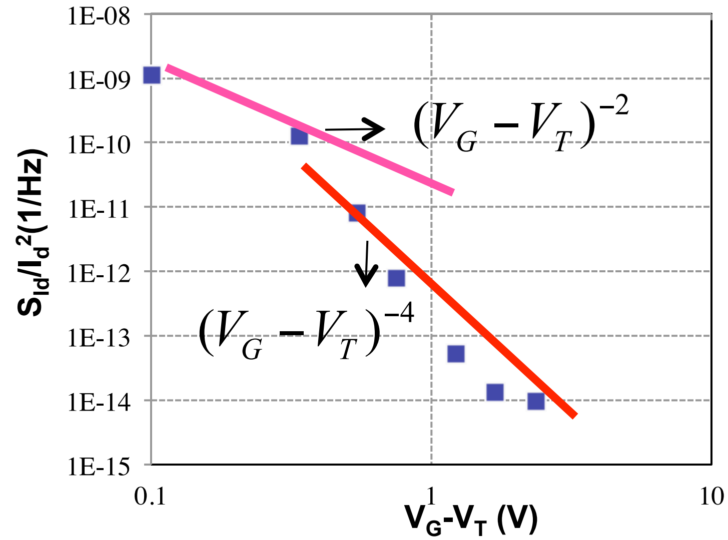
$$S_{I_d} / I_d^2 \propto (\frac{1}{N})^2 \propto (V_{GS} - V_T)^{-2}$$

- Hooge mobility fluctuations

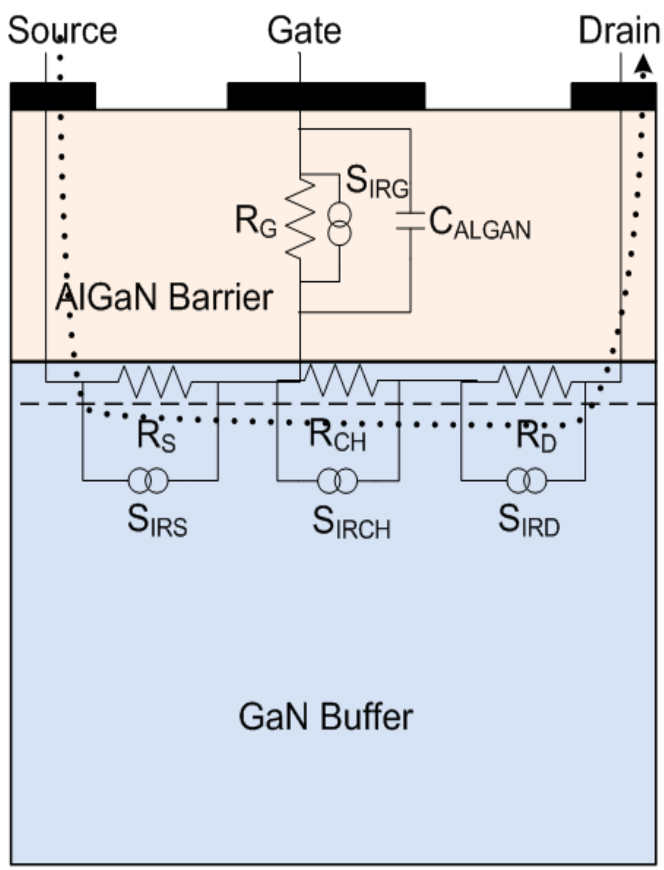
$$S_{I_d} / I_d^2 = \frac{\alpha_H}{Nf} \propto (V_{GS} - V_T)^{-1}$$

For virgin device mobility fluctuations dominate. Carrier number fluctuations dominate on stressed device.





Channel Noise Source Of Stressed Device



$$\frac{S_{ID}}{I_D^2}=\frac{S_{RCH}}{R_{CH}^2}\left(\frac{R_{CH}^2}{(R_S+R_D+R_{CH})^2}\right)+\frac{S_{RD}}{R_D^2}\left(\frac{R_D^2}{(R_S+R_D+R_{CH})^2}\right)+\frac{S_{RS}}{R_S^2}\left(\frac{R_S^2}{(R_S+R_D+R_{CH})^2}\right)$$

Case I: $R_{CH}>(R_S+R_D), S_{R_{CH}}>(S_{R_S}+S_{R_D})$

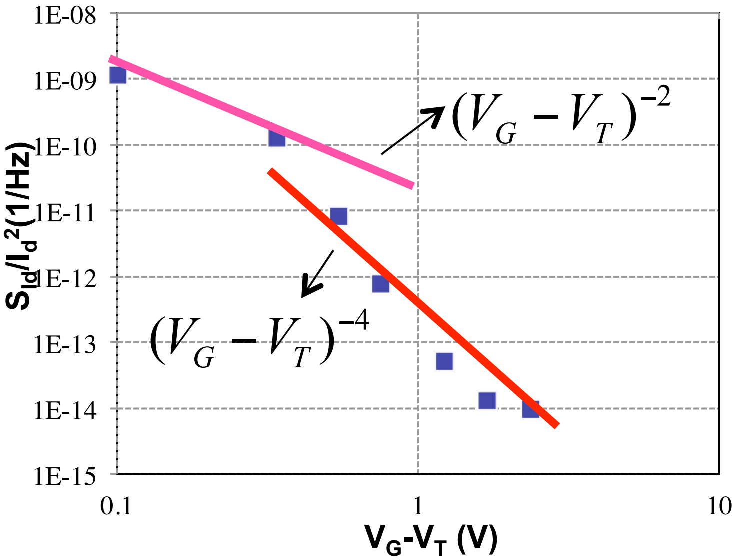
$$\frac{S_{I_D}}{I_D^2}\cong\frac{S_{R_{CH}}}{R_{CH}^2}\propto(V_G-V_T)^{-2}$$

Case II: $(R_S+R_D)>R_{CH}, S_{R_{CH}}>(S_{R_S}+S_{R_D})$

$$\frac{S_{I_D}}{I_D^2}\cong\frac{S_{R_{CH}}}{R_A^2}+\frac{S_{R_A}}{R_A^2}\cong\frac{S_{R_{CH}}}{R_A^2}=\frac{S_{R_{CH}}}{R_{CH}^2}\times\left(\frac{R_{CH}}{R_A}\right)^2\propto(\mathrm{V}_G-V_T)^{-4}$$

Where, $R_A=R_S+R_D, S_{R_A}=S_{R_S}+S_{R_D}$

Channel Noise Source Of Stressed Device



Case III: $R_{CH} > (R_S + R_D), (S_{R_S} + S_{R_D}) > S_{R_{CH}}$

$$\frac{S_{I_D}}{I_D^2} \cong \frac{S_{R_A}}{R_{CH}^2} \propto (V_G - V_T)^2$$

Case IV: $(R_S + R_D) > R_{CH}, (S_{R_S} + S_{R_D}) > S_{R_{CH}}$

$$\frac{S_{I_D}}{I_D^2} \cong \frac{S_{R_A}}{R_A^2} \propto (\mathrm{V}_G - V_T)^0$$

Where, $R_A = R_S + R_D, S_{R_A} = S_{R_S} + S_{R_D}$

Noise information of the channel should be extracted from the first two points.

Hooge Parameter On Channel

At first two point, $R_{CH} > (R_S + R_D), S_{R_{CH}} > (S_{R_S} + S_{R_D})$

$$\frac{S_{I_D}}{I_D^2} \cong \frac{S_{R_{CH}}}{R_{CH}^2} = \frac{\alpha_{CH}}{N_{CH} f} \qquad Where, N_{CH} = C_{AlGaN}(V_{GS} - V_T)$$

Hooge parameter (α_H) changed from ~ 10^{-3} (virgin device) to ~ 10^{-1} (stressed device).

Compared with Silicon MOSFET α_H ranging from 10^{-3} to 10^{-7}.

$$N_t = \frac{S_{I_d} C_{OX}^2 W L f^{\gamma} (V_{GS} - V_T)^2}{q^2 k T I_D^2 \lambda}$$

Nt for stressed device is about 10^{21}cm^{-3}.eV^{-1}. Typical value for Si MOSFET is in the range of 10^{17}~10^{18}cm^{-3}.eV^{-1}

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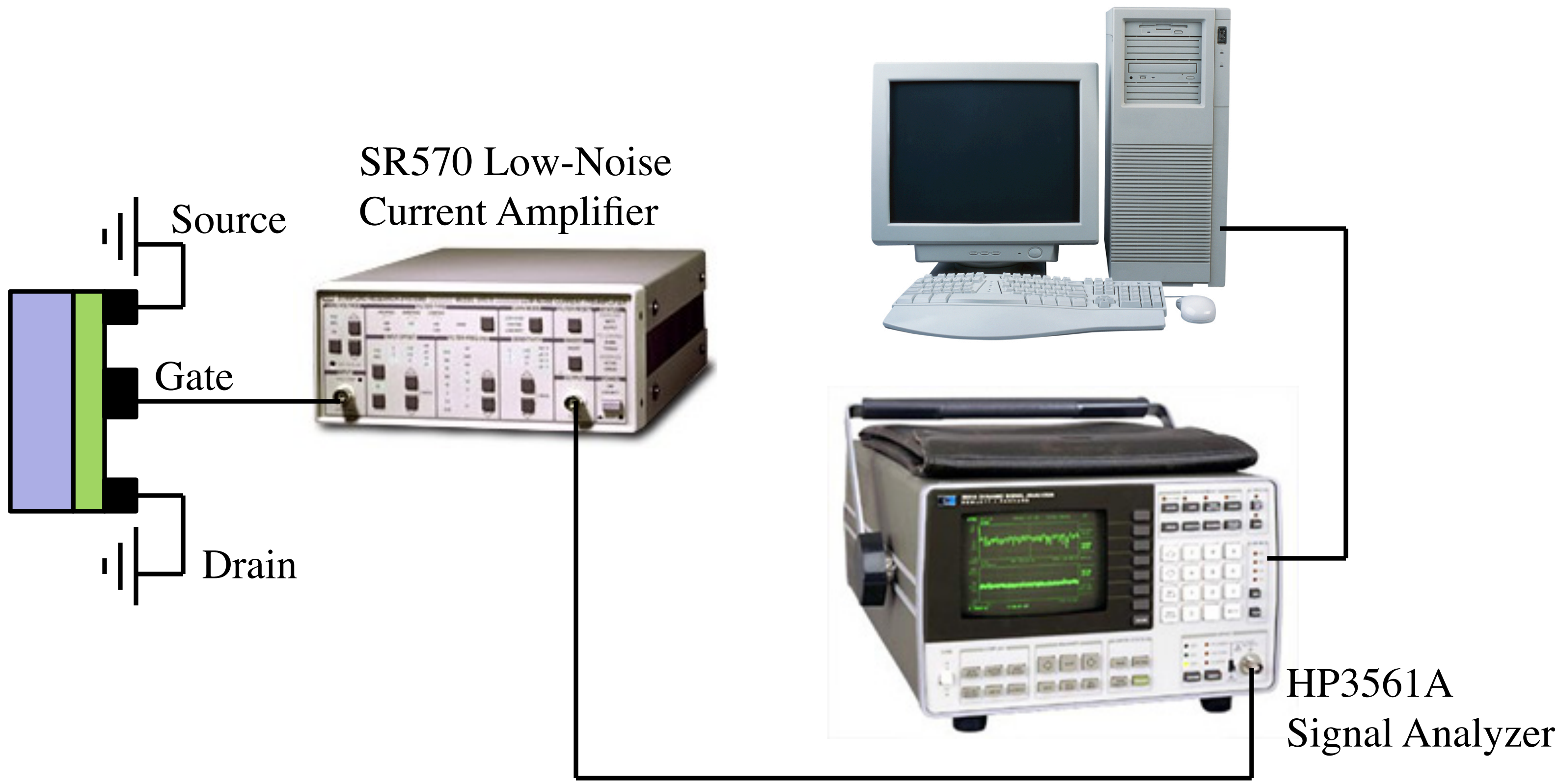
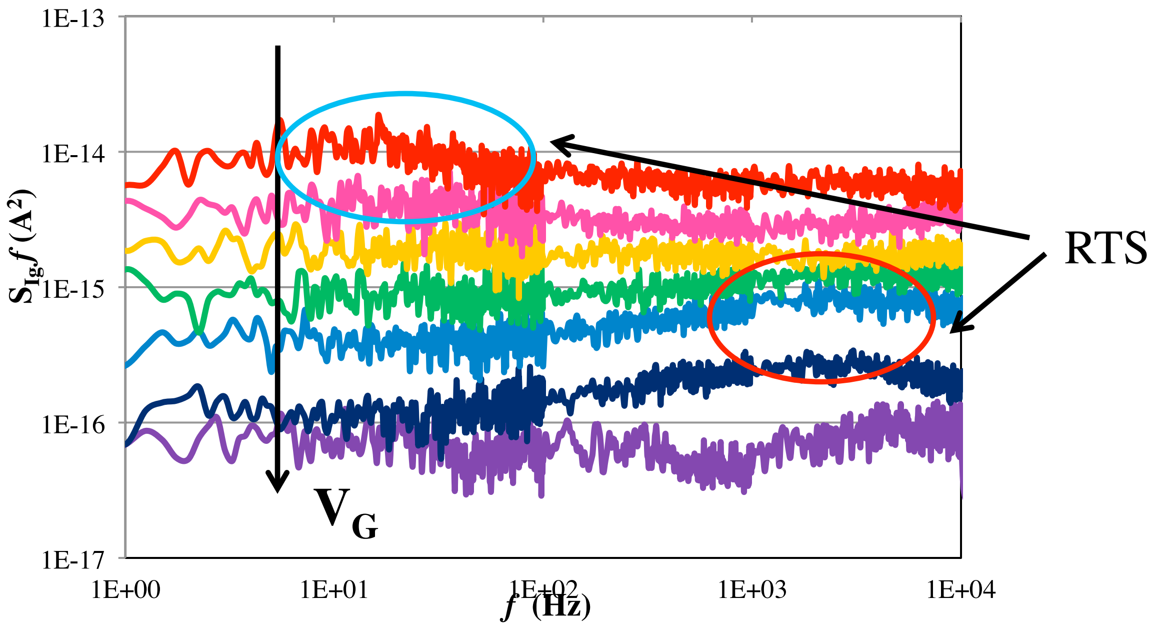
Gate Noise Measurement Setup

Source and drain were grounded.

Gate biased from -3.5V (threshold) to -1V.

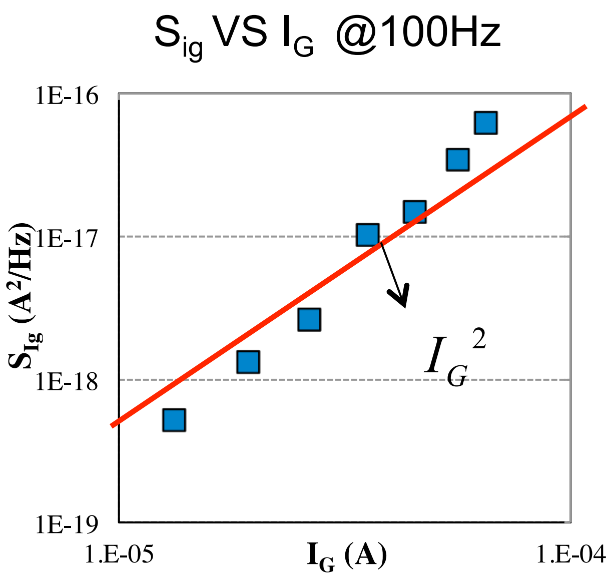


Gate Noise Characteristics



- S_{ig} increase with I_G.
- Unstable Lorentzian with different characteristic frequencies were observed.

Gate Noise Parameter



GNP (Gate Noise Parameter) is defined as

$$GNP \equiv \frac{S_{I_G} f A}{I_G^2}$$

- GNP after stress is around 10^{-13} cm^2. (For $I_G \sim 10^{-6}$A)
- Typical value of GNP for Silicon MOSFET is around 10^{-16} cm^2

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Conclusions

- Degradation happened in both channel and gate stack after off-state stress beyond critical voltage. (Channel degradation was observed for the first time)
- Trap in AlGaN close to interface was generated.
- α_{CH} increased by two decades from 10^{-3} to 10^{-1} indicating important degradation inside the channel.
- RTS in the gate noise was observed on oscilloscope indicating unstable defects in the gate stack..
- Significant increase on I_G shows evidence of degradation inside the gate stack. And GNP of stressed AFRL device is about 10^{-13} cm^2, comparing to 10^{-16} cm^2 of Si MOSFET.

Thank you!